What is claimed is:

1. A data strobe circuit for prefetching M number of N bit data, N and M being a positive integer, comprising:

a data strobe buffering means for generating N number of align control signals based on a data strobe signal;

a synchronizing block having M number of latch blocks, each for receiving N bit data and outputting the N-1 bit data in a parallel fashion in response to N-1 number of the align control signals and one bit prefetched data in response to the remaining align control signals; and

a output block having M number of aligning blocks, each for receiving the N-1 bit data in the parallel fashion, synchronizing the N-1 bit data with the align control signal and outputting the synchronized N-1 bit data as the N-1 bit prefetched data.

2. The data strobe circuit as recited in claim 1, wherein at least one or more align control signals have a period at least twice longer than period of the data strobe signal.

3. The data strobe circuit as recited in claim 1, wherein the synchronizing block includes the M number of latch blocks, each having N number of latches, each for latching one bit data in response to one align control signal.

4. The data strobe circuit as recited in claim 1, wherein the output block includes the M number of aligning blocks, each having N-1 number of aligning units, each for receiving at least one align control signal, synchronizing one bit data with the align control signal and outputting the one bit synchronized data as the one bit prefetched data.

5. The data strobe circuit as recited in claim 1, wherein the N is 4.

6. The data strobe circuit as recited in claim 5, wherein the data strobe dividing means generates first rising and falling data strobe signals and second rising and falling data strobe signals in response to rising and falling edges of the data strobe signal.

7. The data strobe circuit as recited in claim 6, wherein the synchronizing block includes at least one latch block for latching the 4 bit data inputted in response to the first rising and falling data strobe signals and the second rising and falling data strobe signals and outputting one bit latched data in response to the second falling data strobe signal as the one bit prefetched data.

8. The data strobe circuit as recited in claim 7, wherein the output block includes at least one aligning block for receiving the 3 bit data inputted from the latch means in

response to the first falling data strobe signal, the second rising data strobe signal and the second falling data strobe signal and simultaneously outputting the 3 bit synchronized data as the 3 bit prefetched data.

9. The data strobe circuit as recited in claim 6, wherein a rising edge of the first rising data strobe signal corresponds with a rising edge at a first period of the original data strobe signal; a rising edge of the first falling data strobe signal corresponds with a falling edge at a first period of the original data strobe signal; a rising edge of the second rising data strobe signal corresponds with a rising edge at a second period of the original data strobe signal; and a rising edge of the second rising data strobe signal corresponds with a falling edge at a second period of the original data strobe signal.

10. The data strobe circuit as recited in claim 9, wherein the latch block includes:

a first rising latch for latching a first data in response to the rising edge of the first rising data strobe signal;

a first falling latch for latching a second data in response to the rising edge of the first falling data strobe signal;

a second rising latch for latching a third data in response to the rising edge of the second rising data strobe

signal; and

a second falling latch for latching a forth data in response to the rising edge of the second falling data strobe signal.

11. The data strobe circuit as recited in claim 10, wherein the aligning block includes:

a first rising align block for simultaneously outputting the first data latched by the first rising latch block at the point of timing when the forth data is outputted from the second falling latch block;

a first falling align block for simultaneously outputting the second data latched by the first falling latch block at the point of timing when the forth data is outputted from the second falling latch block; and

a second rising align block for simultaneously outputting the third data latched by the second rising latch block at the point of timing when the forth data is outputted from the second falling latch block.

12. The data strobe circuit as recited in claim 11, wherein the first rising align block includes

a first transmission gate for delivering the inputted first datum in response to the rising edge of the first falling data strobe signal;

a first inverter for inverting the first datum outputted from the first transmission gate;

a second inverter for receiving the inverse first datum outputted from the first inverter;

a third inverter circularly connected to the second inverter for latching the first datum outputted from the first inverter;

a second transmission gate for outputting the first datum outputted from the second inverter in response to the rising edge of the second rising data strobe signal;

a forth inverter for inverting the first datum outputted from the second transmission gate;

a fifth inverter for receiving the inverse first datum outputted from the forth inverter;

a sixth inverter circularly connected to the fifth inverter for latching the first datum outputted from the forth inverter; and

a third transmission gate for outputting the first datum outputted from the fifth inverter in response to the rising edge of the second falling data strobe signal.

13. The data strobe circuit as recited in claim 11, wherein the first falling align block includes

a first transmission gate for delivering the inputted second datum in response to the rising edge of the second rising data strobe signal;

a first inverter for inverting the second datum outputted from the first transmission gate;

a second inverter for receiving the inverse second datum

outputted from the first inverter;

a third inverter circularly connected to the second inverter for latching the second datum outputted from the first inverter; and

a second transmission gate for outputting the second datum outputted from the second inverter in response to the rising edge of the second falling data strobe signal.

14. The data strobe circuit as recited in claim 11, wherein the second rising align block includes

a first transmission gate for delivering the inputted third datum in response to the rising edge of the second falling data strobe signal.

15. The data strobe circuit as recited in claim 11, wherein the first rising align block includes

a first transmission gate for outputting the first datum outputted from the fifth inverter in response to the rising edge of the second falling data strobe signal.

16. The data strobe circuit as recited in claim 11, wherein the first falling align block includes

a first transmission gate for outputting the first datum outputted from the fifth inverter in response to the rising edge of the second falling data strobe signal.